AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

~~a plurality of~~ field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying power supply voltages to ~~a plurality of~~ said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements include a plurality of said field effect transistors ~~of said basic cells~~which are not used in performing logic operations of a logic circuit.

Claims 2 - 6 (Cancelled)

7. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

~~a plurality of~~ field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying power supply voltages to ~~a plurality of~~ said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings;

wherein said switch elements include a plurality of field effect transistors ~~of said basic cells and~~ which are discretely arranged in said semiconductor region, and which are not used in performing logic operations of a logic circuit.

8. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

~~a plurality of~~ field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements include a plurality of said field effect transistors ~~of said basic cells~~ which are not used in performing logic operations of a logic circuit, and

wherein a semiconductor region, which is formed within said semiconductor region in a plurality of said basic cells and of a conductivity type opposed to that of said semiconductor region, is electrically connected to said power supply wirings.

9. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

~~a plurality of~~ field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements include a plurality of said field effect transistors ~~of said basic cells~~which are not used in performing logic operations of a logic circuit, and at least one of a pair of semiconductor regions for source and drain of unused field effect transistors of said ~~field effect transistors~~ plurality of basic cells and said power supply wirings are electrically connected.

10. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

~~a plurality of~~ field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements include a plurality of said field effect transistors ~~of said basic cells and~~ which are discretely arranged within said semiconductor region, and which are not used in performing logic operations of a logic circuit, and

wherein a semiconductor region, formed in said semiconductor region of a plurality of basic cells and of a conductivity type opposed to that of said semiconductor region, and said power supply wirings are electrically connected.

11. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

~~a plurality of~~ field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements include a plurality of field effect transistors ~~of said basic cells and~~ which are discretely arranged within said semiconductor region, and which are not used in performing logic operations of a logic circuit, and

wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors of said field effect transistors of said plurality of basic cells and said power supply wirings are electrically connected.

12. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

~~a plurality of~~ field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements include a plurality of said field effect transistors ~~of said basic cells and~~ which are

discretely arranged in said semiconductor region, and which are not used in performing logic operations of a logic circuit, and

wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors arranged between the switch elements ~~discretely arranged in said semiconductor region among said field effect transistors~~ and said power supply wirings are electrically connected.

13. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

~~a plurality of~~ basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

circuits formed of a plurality of said basic cells;

power supply wirings arranged for supplying power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements are built in a predetermined

circuit among said circuits, and include basic cell portions not used in performing logic operations of a logic circuit.

14. (Currently Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

circuits formed of a plurality of said basic cells;

power supply wirings arranged for supplying power supply voltages to said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings, and which are not used in performing logic operations of a logic circuit,

wherein said circuits include a circuit in which said switch elements are built in and the circuit in which said switch elements are not built in.

15. (Previously Presented) A semiconductor device as claimed in claim 13 or 14, wherein a semiconductor region, formed in said semiconductor region of a plurality of said basic cells and of a conductivity type opposed to that of said semiconductor region, and said power supply wirings are electrically connected.

16. (Original) A semiconductor as claim in claim 13 or 14, wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among said field effect transistors and said power supply wirings are electrically connected.

17. (Previously Presented) A semiconductor device as claimed in claim 13 or 14, wherein said circuits are logic circuits and said switch elements are discretely arranged in said semiconductor substrate.

18. (Original) A semiconductor device as claimed in claim 16, wherein said unused field effect transistors are field effect transistors of basic cells not forming logic circuits and said unused basic cells are formed among said switch elements.

19. (Previously Presented) A semiconductor device as claimed in claim 13 or 14, wherein said circuit in which the switch elements are built in is a clock circuit or a flip-flop circuit.

20. (Previously Presented) A semiconductor device as claimed in claim 13 or 14, wherein said switch elements include field effect transistors of said basic cells.

21. (Previously Presented) A semiconductor device as claimed in any one of claims 7 to 14, wherein said basic cells include p-channel type field effect transistors and n-channel type field effect transistors.

22. (Previously Presented) A semiconductor device as claimed in any one of claims 7 to 12, further comprising:

a first wiring layer formed over said switch elements;

a second wiring layer formed over said first wiring layer and having wiring extending in a direction transverse to wiring of said first wiring layer; and

a third wiring layer formed over said second wiring layer and having wiring extending in a direction transverse to wiring of said second wiring layer,

wherein a wiring electrically connected to gate electrodes of said switch elements is formed of wiring of the

third wiring layer and arranged in parallel to said power supply wirings.

23. (Previously Presented) A semiconductor device as claimed in any one of claims 7 to 14, wherein a semiconductor region for power feeding to supply a predetermined voltage to the semiconductor region formed in said semiconductor substrate is formed in a region between an internal circuit region where a plurality of said basic cells are arranged and a peripheral circuit region at an external side of said internal circuit region.

24. (Original) A semiconductor device as claimed in claim 23, wherein a wiring for supplying the predetermined voltage to said semiconductor region for power feeding is arranged to surround said internal circuit region.

25. (Previously Presented) A semiconductor device as claimed in claim 24, wherein the wiring for supplying the predetermined voltage to said semiconductor region for power feeding is electrically connected to a terminal for testing via an external terminal of the semiconductor device.

26. (Previously Presented) A semiconductor device as claimed in claim 24, wherein the wiring for supplying the

predetermined voltage to said semiconductor region for power feeding is electrically connected to wiring for power feeding arranged like a lattice within said internal circuit region.

27. (Previously Presented) A semiconductor device as claimed in any one of claims 1 and 7 to 14, wherein said switch elements are turned ON in a normal operation period of the semiconductor device and a power supply voltage is applied from said power supply wirings to the semiconductor region formed in said semiconductor substratec and said switch elements are turned OFF in a testing or waiting period of the semiconductor device and a voltage different from said power supply voltage is applied to said semiconductor region.

28. (Previously Presented) A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have a conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged on said semiconductor substrate;

first field effect transistors formed in said first semiconductor region as field effect transistors of said basic cells;

second field effect transistors formed in said second semiconductor region as field effect transistors of said basic cells and to have a conductivity type opposed to that of said first field effect transistors;

a first power supply wiring connected to said first field effect transistors;

a second power supply wiring connected to said second field effect transistors to supply a potential which is relatively lower than a potential of said first power supply wiring;

first switch elements provided between said first semiconductor region and said first power supply wiring; and

second switch elements provided between said second semiconductor region and said second power supply wiring,

wherein said first switch elements are formed of a plurality of the first field effect transistors in said basic cells and discretely arranged within said first semiconductor region, [[and]]

wherein said second switch elements are formed of a plurality of second field effect transistors in said basic cells and discretely arranged within said second semiconductor region, and

wherein the first and second pluralities of field effect transistors are not used in performing logic operations of a logic circuit.

29. (Currently Amended) A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have a conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged on said semiconductor substrate;

first field effect transistors formed in said first semiconductor region as field effect transistors of said basic cells;

second field effect transistors formed in said second semiconductor region as field effect transistors of said basic cells and to have a conductivity type opposed to that of said first field effect transistors;

a first power supply wiring connected to said first field effect transistors;

a second power supply wiring connected to said second field effect transistors to supply a potential which is relatively lower than that of said first power supply wiring;

first switch elements provided between said first semiconductor region and said first power supply wiring; and

second switch elements provided between said second semiconductor region and said second power supply wiring,

wherein said first switch elements include the first field effect transistors in predetermined basic cells among said plurality of basic cells and which are not used in performing logic operations of a logic circuit,

wherein said second switch elements includethe second field effect transistors in predetermined basic cells among said plurality of said basic cells and which are not used in performing logic operations of a logic circuit,

wherein a region formed in said first semiconductor region in a plurality of said basic cells electrically connects the semiconductor region of the conductivity type opposed to that of said first semiconductor region and said first power supply wiring, and

wherein a region formed in said second semiconductor region in a plurality of basic cells electrically connects the semiconductor region of the conductivity type opposed to that of said second semiconductor region and said second power supply wiring.

30. (Currently Amended) A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have a conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged on said semiconductor substrate;

first field effect transistors formed in said first semiconductor region as field effect transistors of said basic cells;

second field effect transistors formed in said second semiconductor region as field effect transistors of said basic cells and to have a conductivity type opposed to that of said first field effect transistors;

a first power supply wiring connected to said first effect transistors;

a second power supply wiring connected to said second field effect transistors to supply a potential relatively lower than that of said first power supply wiring;

first switch elements provided between said first semiconductor region and said first power supply wiring; and

second switch elements provided between said second semiconductor region and said second power supply wiring,

wherein said first switch elements include the first field effect transistors in predetermined basic cells among said plurality of basic cells and which are not used in performing logic operations of a logic circuit,

wherein said second switch elements include the second field effect transistors in predetermined basic cells among said plurality of basic cells and which are not used in performing logic operations of a logic circuit,

wherein at least one of a pair of semiconductor regions for source and drain of unused first field effect transistors among said first field effect transistors is electrically connected to said first power supply wiring, and

wherein at least one of a pair of semiconductor regions for source and drain of unused second field effect transistors among said second field effect transistors is electrically connected said second power supply wiring.

31. (Currently Amended) A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have a conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged on said semiconductor substrate;

first field effect transistors formed in said first semiconductor region as field effect transistors of said basic cells;

second field effect transistors formed in said second semiconductor region as field effect transistors of said basic cells and to have a conductivity type opposed to that of said first field effect transistors;

a first power supply wiring connected to said first field effect transistors;

a second power supply wiring connected to said second field effect transistors to supply a potential relatively lower than that of said first power supply wiring;

first switch elements provided between said first semiconductor region and said first power supply wiring; and

second switch elements provided between said second semiconductor region and said second power supply wiring

wherein said first switch elements include the first field effect transistors in predetermined basic cells among said plurality of basic cells and are discretely arranged in said first semiconductor region, said first field effect transistors of said first switch elements not being used in performing logic operations of a logic circuit,

wherein said second switch elements include the second field effect transistors in predetermined basic cells amongsaid plurality of basic cells and are discretely arranged in said semiconductor region, said second field effect transistors of said second switch elements not being used in performing logic operations of a logic circuit,

wherein a region formed in said first semiconductor region in a plurality of said basic cells electrically connects the semiconductor region of the conductivity type opposed to that of said first semiconductor region and said first power supply wiring, and

wherein a region formed in said second semiconductor region in a plurality of said basic cells electrically connects the semiconductor region of the conductivity type opposed to that of said second semiconductor region and said second power supply wiring.

32. (Currently Amended) A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a second semiconductor region formed in said semiconductor substrate to have a conductivity type opposed to that of said first semiconductor region;

a plurality of basic cells regularly arranged on said semiconductor substrate;

first field effect transistors formed in said first semiconductor region as field effect transistors of said basic cells;

second field effect transistors formed in said second semiconductor region as field effect transistors of said basic cells and to have channel conductivity type opposed to that of said first field effect transistors;

a first power supply wiring connected to said first field effect transistors;

a second power supply wiring connected to said second field effect transistors to supply a potential relatively lower than that of said first power supply wiring;

first switch elements provided between said first semiconductor region and said first power supply wiring; and

second switch elements provided between said second semiconductor region and said second power supply wiring,

wherein said first switch elements include the first field effect transistors in predetermined basic cells among said plurality of basic cells and are discretely arranged in said first semiconductor region, said first field effect transistors of said first switch elements not being used in performing logic operations of a logic circuit,

wherein said second switch elements include the second field effect transistors in predetermined basic cells among said plurality of basic cells and are discretely arranged in said second semiconductor region, said second field effect transistors of said second switch elements not being used in performing logic operations of a logic circuit,

wherein at least one of a pair of semiconductor regions for source and drain of unused first field effect transistors among said first field effect transistors is electrically connected to said first power supply wiring, and

wherein at least one of a pair of semiconductor regions for source and drain of unused second field effect transistors

among said second field effect transistors is electrically connected to said second power supply wiring.

33. (Previously Presented) A semiconductor device, comprising:

first and second semiconductor regions formed in a peripheral circuit region of a semiconductor substrate;

a plurality of cells for input/output circuits regularly arranged in the peripheral circuit region of said semiconductor substrate;

a plurality of field effect transistors for input/output circuits arranged in each of a plurality of cells for input/output circuits and formed in said first and second semiconductor regions;

power supply wiring arranged for supplying a power supply voltage to a plurality of said field effect transistors for input/output circuits; and

switch elements provided between the second semiconductor region in said peripheral circuit region and said power supply wiring,

wherein an output circuit electrically connected to an external terminal includes field effect transistors for input/output circuits in said first semiconductor region and an input circuit electrically connected to an external terminal includes field effect transistors for input/output circuits in said second semiconductor region, and

wherein said switch elements include field effect transistors not used for the input circuit among the field effect transistors for input/output circuits in said second semiconductor region.

34. (Previously Presented) A semiconductor device, comprising:

a semiconductor region formed in a peripheral circuit region of a semiconductor substrate;

a plurality of cells for input/output circuits regularly arranged in the peripheral circuit region of said semiconductor substrate;

a plurality of field effect transistors for input/output circuits arranged in each of a plurality of cells for input/output circuits and formed in said semiconductor region;

power supply wiring arranged for supplying a power supply voltage to a plurality of said field effect transistors for input/output circuits; and

switch elements provided between the semiconductor region in peripheral circuit region and said power supply wiring,

wherein said peripheral circuit region includes an external region to arrange field effect transistors for input/output circuits of relatively higher threshold voltage and an internal region to arrange field effect transistors for

input/output circuits of relatively lower threshold voltage, and

wherein said switch elements include field effect transistors not used for input circuit among the field effect transistors for input/output circuits in said internal region.

35. (Previously Presented) A semiconductor device as claimed in claim 34, wherein an output circuit includes a field effect transistor for input/output circuit in said external region and an input circuit includes a field effect transistor for input/output circuits in said internal region.

36. (Previously Presented) A semiconductor device as claimed in claim 33, 34 or 35, wherein a gate insulation film of the field effect transistor of said output circuit is thicker than a gate insulation film of the field effect transistor of said input circuit.

37. (Previously Presented) A semiconductor device as claimed in claim 33, 34, or 35, wherein wiring connected to the gate electrodes of the field effect transistors of said switch elements is arranged to surround said internal region.

38. (Previously Presented) A semiconductor device as claimed in any one of claims 33 to 35, wherein at least one of a pair of semiconductor regions for source and drain of the

field effect transistors unused for said input/output circuits is electrically connected to said power supply wiring to form a capacitance element.

39. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate;

(b) forming [[a]] switch elements arranged for electrically connecting and disconnecting a semiconductor region formed on said semiconductor substrate and a power supply wiring of the semiconductor device with field effect transistors of predetermined basic cells among said plurality of basic cells, which field effect transistors are not used in performing logic operations of a logic circuit; and

(c) forming a plurality of circuits with predetermined basic cells among said plurality of basic cells.

40. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate;

(b) forming switch elements arranged for electrically connecting and disconnecting a semiconductor region formed on said semiconductor substrate and a power supply wiring of the

semiconductor device with field effect transistors of predetermined basic cells among said plurality of basic cells;

(c) forming a plurality of circuits with predetermined basic cells among said plurality of said basic cells, said field effect transistors not being used in performing logic operations of a logic circuit; and

(d) allocating a contact hole arranged for electrically connecting at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among field effect transistors of said basic cells and said power supply wiring.

41. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

(a) regularly allocating a plurality basic cells on a semiconductor substrate;

(b) forming a switch element arranged for electrically connecting and disconnecting a semiconductor region formed on said semiconductor substrate and a power supply wiring of the semiconductor device with a field effect transistor of a predetermined basic cell among said plurality of said basic cells said field effect transistor not being used in performing logic operations of a logic circuit; and

(c) forming a plurality of circuits with predetermined basic cells among said plurality of basic cells,

wherein said switch element is built in predetermined circuit among said plurality of said circuits in step (c).

42. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate; and

(b) forming a plurality of circuits with predetermined basic cells among said plurality of basic cells,

wherein a switch element is built in a predetermined circuit among a plurality of said circuits,

said switch element including a field effect transistor of a basic cell of said predetermined circuit, said field effect transistor not being used in performing logic operations of a logic circuit and being provided between a power supply wiring and a semiconductor region in which field effect transistors of other basic cells of said predetermined circuit are formed.

43. (Previously Presented) A semiconductor device as claimed in claim 8, wherein a capacitance element is formed of said semiconductor region and a semiconductor region of a conductivity type opposed to that of said semiconductor region.

44. (Previously Presented) A semiconductor device as claimed in claim 9, 11 or 12, wherein a capacitance element is formed of said semiconductor region and at least one of a pair of semiconductor regions for source and drain of said unused field effect transistors.

45. (Previously Presented) A semiconductor device as claimed in any one of claims 7 to 12, wherein a logic circuit is formed using said basic cells and said logic circuit is formed among the basic cells including said switch elements.

46. (Currently Amended) A semiconductor device claimed in claim 9, 11, or 12, wherein a logic circuit is formed using said basic cells, a field effect transistor having said one pair of semiconductor regions is a field effect transistor of an unused basic cell not forming a logic circuit, and said logic circuit and unused basic cell[[s]] are formed among the basic cells including said switch elements.